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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,191	01/14/2002	Tsutomu Hatakeyama	218102US2	6192

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,191	HATAKEYAMA, TSUTOMU	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9 and 10* is/are rejected.

7)☒ Claim(s) *4 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/14/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. Claims 1-10 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-7, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar (U.S. Patent 5,675,540 hereafter referred to as Roohparvar) in

view of Matsumoto et al. (U.S. Patent 5,278,839 hereafter referred to as Matsumoto.)

As per claim 1:

Roohparvar substantially teach the invention. Roohparvar teaches:

A semiconductor device having a function verification capability [abstract, column 1, line 9] comprising:

- an internal verification block [abstract, fig.1, item 50, column 2, line 41] receiving and then storing first input value [fig.1, item 30];

- a target verification block [fig. 1, item 104] corresponding to the internal verification block [abstract, fig.1, item 50], both values being for use in an operation verification according to execution of internal verification instructions during the operation verification [col.7, lines 47-50, col. 17, lines 1-4], and

- supplying the first input data to the target verification block instead of a second input data being for use in a normal operation [fig.1, from item 102].

Roohparvar does not explicitly teach:

- a cycle value being a timing to supply the first input value to a target verification block.

However, Roohparvar does disclose a similar capability of:

- verification cycle [col.3, line 2], pre-programming cycle [col.3, line 5] and erase cycle [col.3, line 61] for the internal data verification test mode.

In addition, Matsumoto explicitly teaches:

- A semiconductor integrated circuit has the function of self-checking [verification] defective bits [abstract, fig. 1, col. 1, lines 54-55];

comprising:

- a timing for self-repairing defective addresses in a memory cell array with timing generation means [fig.1, item 10, col.1, lines 66-68].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to apply the a timing for self-repairing defective addresses in a memory cell array with timing

generation means taught by Matsumoto in conjunction with the internal verification block as disclosed by Roohparvar in order to verify a function relating to input data caused by an external interrupt. One of ordinary skill in the art would have been motivated to do so to improve the system interconnectivity's data throughput, data availability, and data access.

As per claim 2:

Roohparvar further teaches:

- a plurality of the first input data and the corresponding cycle values are set to the internal verification block continuously [fig. 1, item 22, col. 2, lines 30-33].

In addition, Matsumoto teaches each of the first input data is supplied to the target verification block every a lapse of the corresponding cycle value [col.2, lines 46-49, col. 3, lines 1-3].

As per claim 3:

Roohparvar further teaches:

- the internal verification block comprises: a register storing the first input value [fig.1, item 26, col.2, lines 43-45];

- a counter[fig.1, item 52] to which the cycle value is set, decrementing this cycle value;

- a detector detecting that the value of the counter becomes zero [fig.6, item 102, col. 12, lines 25-31; and

- a multiplexer selecting the first input data stored in the register instead of the second input data for use in the normal operation when the detector detects that the value of the counter becomes zero, and supplying the selected one to the target verification block [fig.1, item 104].

As per claims 5-7:

Roohparvar further teaches:

- the internal verification instructions are described in a verification program to verify the operation of the target verification block and executed in synchronization with pipeline operation [col.2, line 63 through col.3, line 6].

As per claims 9-10:

Roohparvar does not explicitly teach:

- a plurality of the internal verification blocks and the target verification blocks, and each internal verification block corresponds to each target verification block in a one-to-one correspondence between them. However, Roohparvar does disclose a similar capability of:

- an input/output pad [302] is connected to circuit elements data read path [304] and a data write path [306] to a memory array [col.5, line 66 through col.6, line 3].

- a plurality of input/output lines and one data input/output circuit [300] associated with each data input/output line [col.6, lines 5-9].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made first, to realize the Roohparvar's method of non-volatile memory having internal data verification test mode to comprising a plurality of input/output lines and one data input/output circuit [300] associated with each data input/output line as being a plurality of the internal verification blocks and the target verification blocks, and each internal verification block corresponds to each target verification block in a one-to-one correspondence between

them as claimed by Applicant. This is because both inventions are dealing with semiconductor having internal verification test.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to provide the data transmission system with plurality of communication devices and peripheral with a mechanism to enhance data transfer means for data recovery process via the state logic or state machine capability or clock signaling.

Allowable Subject Matter

4. Claims 4, 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703)305-9408 **[NOTE: After approximately October 15, 2004, I can be reached at the new number (571) 272-3660]**. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
9/16/04